What is Claimed is:

1. A packaged semiconductor device, comprising:

a semiconductor die;

a substrate, with the semiconductor die disposed therein;

a plurality of leads coupled to the semiconductor die;

an encapsulant enclosing the semiconductor die and plurality of leads; and

the encapsulant operable to shunt thermal capacitance and thermal resistance away from the semiconductor die.

2. The packaged semiconductor device as recited in Claim 1, further comprising an I/O common terminal, at least one input terminal and at least one output terminal, coupled to the semiconductor die.

3. The packaged semiconductor device as recited in Claim 2, wherein the input terminal(s) and output terminal(s) are positioned orthogonal to the I/O common terminal.

4. The packaged semiconductor device as recited in Claim 3, wherein the semiconductor die is positioned above the I/O common terminal.

5. The packaged semiconductor device as recited in Claim 4, wherein the encapsulant forms a substantially hexagonal structure surrounding the I/O common terminal, input terminal(s), and output terminal(s), essentially at right angles with respect to the substrate.

6. The packaged semiconductor device as recited in Claim 5, further comprising a lead-frame for coupling the input terminal(s) to a circuit and the output terminal(s) to a circuit.

7. The packaged semiconductor device as recited in Claim 6, wherein the portion of the lead-frame coupled to each of the input terminal(s) and output terminal(s) possess exposed dovetailed side edges operable to allow epoxy to lock on the sides and top of the exposed edges.

8. The packaged semiconductor device as recited in Claim 3, further comprising an end surface of the input terminal(s) being positioned adjacent and parallel to the side surface of the I/O common terminal, and an end surface of the output terminal(s) being positioned adjacent and parallel to the opposing side surface of the I/O common terminal, said end surfaces being shaped so as to minimize parasitic capacitance.

9. The packaged semiconductor device as recited in Claim 8, further comprising a rounded shape on the end surface of the input terminal(s) positioned adjacent and parallel to the side surface of the I/O common terminal, and on the end surface of the output terminal(s) positioned adjacent and parallel to the opposing side surface of the I/O common terminal.

10. The packaged semiconductor device as recited in Claim 8, further comprising length and width dimensions of approximately .079 millimeters and .065 millimeters and a height dimension of approximately .032 millimeters.

11. The packaged semiconductor device as recited in Claim 8, further comprising an operating frequency range from DC to 10 gigahertz.

12. The packaged semiconductor device as recited in Claim 8, further comprising use in a surface mount assembly.

13. The packaged semiconductor device as recited in Claim 8, further comprising use in an integrated circuit.

14. The packaged semiconductor device as recited in Claim 8, further comprising use in an amplifier gain stages.

15. The packaged semiconductor device as recited in Claim 8, further comprising metallization, including a first and second metallization strip, as the means of coupling the input terminal(s) and the output terminal(s) to the semiconductor die.

16. The packaged semiconductor device as recited in Claim 15, further comprising a path length from input terminal to the output terminal, of a fraction of the wavelength for which frequency the semiconductor device is designed.

17. The packaged semiconductor device as recited in Claim 8, further comprising bond wires as the means of coupling the input terminal(s) and the

output terminal(s) to the semiconductor die, the input terminal being coupled to a first end of a first bond wire, a second end of the first bond wire being coupled to the semiconductor die, a first end of a second bond wire being coupled to the semiconductor die, a second end of the second bond wire being coupled to the output terminal.

18. The packaged semiconductor device as recited in Claim 17, further comprising a path length from the input terminal to the output terminal of a fraction of the wavelength for which frequency the semiconductor device is designed.

19. The packaged semiconductor device as recited in Claim 1, further comprising a controlled dielectric constant encapsulant operable to provide improved unit-to-unit and run-to-run package parasitic consistency.

20. The packaged semiconductor device as recited in Claim 1, further comprising a light emitting semiconductor as the semiconductor die.

21. The packaged semiconductor device as recited in Claim 20, further comprising a light emitting diode as the light emitting semiconductor.

22. The packaged semiconductor device as recited in Claim 20, further comprising a substantially clear epoxy material as the encapsulant.

23. The packaged semiconductor device as recited in Claim 20, further comprising a cathode and an anode as the plurality of leads.

24. The packaged semiconductor device as recited in Claim 23, further comprising the positioning of the cathode and the anode opposite to each other.

25. The packaged semiconductor device as recited in Claim 24, further comprising an encapsulant with a substantially hexagonal structure around the cathode and the anode essentially at right angles with respect to the substrate.

26. The packaged semiconductor device as recited in Claim 23, further comprising a portion of a conductive lead-frame as the cathode.

27. The packaged semiconductor device as recited in Claim 23, further comprising a shaped end surface of the cathode operable to minimize parasitic capacitance.

28. The packaged semiconductor device as recited in Claim 27, further comprising a rounded shape on the end surface of the cathode.

29. The packaged semiconductor device as recited in Claim 23, further comprising metallization as the cathode coupling means to the semiconductor die.

30. The packaged semiconductor device as recited in Claim 23, further comprising a bond wire as the means of coupling the cathode to the semiconductor die, a first end of the bond wire being coupled to the cathode and a second end of the bond wire being coupled to the semiconductor die.

31. The packaged semiconductor device as recited in Claim 23, further comprising a portion of a conductive lead-frame as the anode.

32. The packaged semiconductor device as recited in Claim 23, further comprising a shaped end surface of the anode operable to minimize parasitic capacitance.

33. The packaged semiconductor device as recited in Claim 32, further comprising a rounded shape on the end surface of the anode.

34. The packaged semiconductor device as recited in Claim 23, further comprising metallization as the anode coupling means to the semiconductor die.

35. The packaged semiconductor device as recited in Claim 23, further comprising a bond wire as the means of coupling the anode to the semiconductor die, a first end of the bond wire being coupled to the anode and a second end of the bond wire being coupled to the semiconductor die.

36. The packaged semiconductor device as recited in Claim 23, further comprising a bond wire as the means of coupling the anode to the semiconductor die, a first end of the bond wire being coupled to the anode and a second end of the bond wire being coupled to the semiconductor die.

37. The packaged semiconductor device as recited in Claim 20, further comprising being adapted for use in an integrated circuit.

38. The packaged semiconductor device as recited in Claim 20, further comprising being adapted for use in a surface mount assembly.

39. The packaged semiconductor device as recited in Claim 20, having length and width dimensions of approximately .079 millimeters and .050 millimeters and a height dimension of approximately .032 millimeters.

40. A packaged semiconductor device, comprising:

a light emitting semiconductor, a substrate, an anode, a cathode and an encapsulant material;

the light emitting semiconductor being disposed in the substrate;

a means of coupling the anode to the light emitting semiconductor;

a means of coupling the cathode to the light emitting semiconductor;

a substantially clear encapsulant for encapsulating the light emitting semiconductor, the encapsulant formed of a substantially hexagonal structure around the anode and the cathode with respect to the substrate, the encapsulant material acting as a thermal shunt to ground operable to decrease thermal capacitance and thermal resistance.

41. The packaged semiconductor device as recited in Claim 40, adapted for use in a surface mount assembly.

42. A packaged semiconductor device, comprising:

a semiconductor die, a substrate and a plurality of leads;

the semiconductor die being disposed in the substrate;

a coupling means from the plurality of leads to the semiconductor die for providing low capacitance electrical connections which supports device functionality; and

an encapsulation material surrounding the semiconductor die, plurality of leads and coupling means, the encapsulation material making contact with the substrate operable to allow direct dissipation shunting to thermal ground.

43. The packaged semiconductor device as recited in Claim 42, adapted for use in a surface mount assembly.

44. The packaged semiconductor device as recited in Claim 42, further comprising a controlled dielectric constant material for the encapsulation material operable to provide improved unit-to-unit and run-to-run package parasitic consistency.

45. A method of assembling a semiconductor device package, comprising:

disposing a semiconductor die in a substrate;

positioning a plurality of leads on opposing sides of the semiconductor die;

coupling the plurality of leads to the semiconductor die;

encapsulating the semiconductor die and plurality of leads in an encapsulant; and

forming and configuring the encapsulant so as to allow direct dissipation shunting to thermal ground.

46. The method of assembling a semiconductor device package as recited in Claim 45, further comprising shaping the ends of the plurality of leads in a substantially rounded form operable to minimize parasitic capacitance.

47. The method of assembling a semiconductor device package as recited in Claim 45, further comprising a light emitting semiconductor as the semiconductor die.

48. The method of assembling a semiconductor device package as recited in Claim 45, further comprising a cathode and an anode as the plurality of leads.

49. The method of assembling a semiconductor device package as recited in Claim 45, further comprising a substantially clear material as the encapsulant.

50. The method of assembling a semiconductor device package as recited in Claim 45, further comprising the encapsulant having a substantially hexagonal structure essentially at right angles with respect to substrate operable to decrease thermal capacitance and thermal resistance.